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EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,024	MORRISON ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,19,21-27,29-64,66 and 67* is/are rejected.

7)☒ Claim(s) *10-18,20,28,49-51 and 65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/09/02 & 09/17/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 09/17/03 in application 10/041,024.

Claim Rejections - 35 USC § 112

2.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 40-61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 40, line 6, "if the processors' results are equal and indicate that the data is erroneous" is not clearly understood what results are equal? And how to determine data erroneous? Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-9, 19, 21-27, 29-48, 52-64, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAuliffe et al. (U.S. Patent 6,367,047 hereafter referred to as McAuliffe) in view of Bruckert et al. (U.S. Patent 5,153,881 hereafter referred to as Bruckert).

As per claim 1:

McAuliffe substantially teach the invention. McAuliffe teaches:

- A data processing system [abstract, fig. 1], comprising:

- a host computer system [col. 3, lines 25];

- an interconnect coupled to the host computer system [col. 3, fig. 1];

- a storage array coupled to the interconnect and configured to store data received from the host computer system over the interconnect [fig. 1, col. 3, line 23];

- a data integrity device coupled to the interconnect and comprising at least one processor [fig. 1, col. 3, lines 24-25];

- first and second levels of error protection for the data [abstract, col. 3, lines 15-20].

McAuliffe does not explicitly teach:

- data integrity device is configured to be enabled and disabled.

However, McAuliffe does disclose capability of:

- A multi-level error detection and correction technique for data stored on storage medium [abstract, fig. 1, col. 2, lines 39-47] comprising capability of:

- a data integrity in data recording/recovery devices [col. 1, lines 38-40];

- "VALID/NOT VALID" data tracking and configuring in responding to error detection and correction process of the device [col. 5, lines 65 through col. 7, line25].

In addition, Bruckert explicitly teaches:

- Error processing in a fault tolerant computing system [abstract, fig. 1, col. 1, lines 5-10];

comprising:

- allocating source of error and enable/disable (i.e., handle/disable) a processor and executing data processor [col. 1, line 50 through col. 2, line7].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply the allocating source of error and enable/disable (i.e., handle/disable) a processor and executing data processor as taught by Brucket in conjunction with "VALID/NOT VALID" data tracking and configuring in responding to error detection and correction process of the device as disclosed by McAuliffe in order to ensuring the memory location error detected, corrected, and replaced in proper and efficient manner via such integrity device or ***firewall***. One of ordinary skill in the art would have been motivated to do so to improve and enhance the data processing and/or data integrity, data recovery time, memory access, memory availability and memory integrity.

As per claims 2-5:

McAuliffe does not explicitly teach:

- comparison of first and second check sum.

However, McAuliffe does disclose capability of:

- A multi-level error detection and correction technique for data stored on storage medium [abstract, fig. 1, col. 2, lines 39-47] comprising capability of:

- CRC packet generation and ECC process [col. 3, lines 35-62].

In addition, Bruckert explicitly teaches:

- Error processing in a fault tolerant computing system [abstract, fig. 1, col. 1, lines 5-10];

comprising:

- ECC comparison capability to support the data processing error detection and correction [col. 12, lines1-66].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to realize both McAuliffe and Bruckert's CRC and ECC error detection and correction means do include the check sum comparison feature. This is because the CRC and ECC do use and perform data or bits within data packet to calculate and check for errors caused by data transmission. By utilizing this approach, data can easily track and correct to enhance its operation.

As per claim 6:

McAuliffe further teaches:

- data is encoded with an error correcting code, wherein as part of the first data integrity operation the data integrity device is configured to verify and correct the data using the error correcting code [col. 3, lines 35-53];

In addition, Bruckert explicitly teaches:

- Error processing in a fault tolerant computing system [abstract, fig. 1, col. 1, lines 5-10];

comprising:

- data is encoded with an error correcting code, wherein as part of the first data integrity operation the data integrity device is configured to verify and correct the data using the error correcting code [col. 17, line 66 through col. 18, line 5 and col. 22, lines 55-65].

As per claim 7-9:

McAuliffe further teaches:

- data integrity device is configured to perform the first and second data integrity operation on the data as the data is written to the storage array [abstract, fig. 1] (i.e., **first and second levels of error protection for the data or multi-level error detection and correction [col. 3, lines 15-20].**

As per claims 19 and 21:

McAuliffe does not explicitly teach:

- array controller to manage the RAID array.

However, McAuliffe does disclose capability of:

- A multi-level error detection and correction technique for data stored on storage medium [abstract, fig. 1, col. 2, lines 39-47] comprising capability of:

- a storage array coupled to the interconnect and configured to store data received from the host computer system over the interconnect [fig. 1, col. 3, line 23];

In addition, Bruckert explicitly teaches:

- Error processing in a fault tolerant computing system [abstract, fig. 1, col. 1, lines 5-10];

comprising:

- memory array and its memory controller used to support the error detection and correction process [col. 6, lines 25-58 and col. 14, lines 60-66].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to realize both McAuliffe and Bruckert's memory and its memory

controller would have included such RAID memory family. This is because RAID memory is notorious well known in the computing arena and is available and readily for use within the data error detection and correction system. For example, RAID memory is widely within the Iwatani's invention titled "DISC Array Apparatus Checking and Restructuring Data Read From Attached DISC Drives including plurality of RAIDs memory array, US Patent 6,023,780.

As per claims 22-25:

McAuliffe further teaches:

- a file system running on the host system [col. 2, lines 43-47];
- memory configured to store instructions [col. 11, lines 57 through col. 12, lines 20];
- host system is configured to update the instructions [col. 11, lines 57 through col. 12, lines 20];
- memory configured to store instructions for performing diagnostic (i.e., verifying data) tests [col. 10, lines 37-51].

In addition, Bruckert explicitly teaches:

- a file system running on the host system [col. 6, lines 5-24];

- memory configured to store instructions [col. 6, lines 25-58];

- host system is configured to update the instructions [col. 11, lines 51 through col. 12, lines 7];

- memory configured to store instructions for performing diagnostic tests [col. 14, lines 60 through col. 15, lines 10].

As per claims 26-27 and 29-32:

McAuliffe further teaches:

- memory configured to buffer the data [col. 2, lines 43-46];

- a plurality of data packets, wherein the data is a first data packet [col. 2, lines 45-47];

- a plurality of data packets, wherein the data comprises the plurality of data packets in the write [col. 3, lines 35-45];

- store a result of the data integrity operation in the memory [col. 10, lines 37-51].

- a packet identification and a time stamp into the packet (i.e., file mark, end-of data marks, etc…) [col. 4, lines 29-40].

- configured to provide its associated device identification if the data integrity device provides an error indication (i.e., packet error recovery indicators) [col. 8, lines 59-67].

As per claims 33-36:

McAuliffe does not explicitly teach:

- in/out of band error indications and data integrity device configured to be inserted or removed from data processing system.

However, McAuliffe does disclose capability of:

- A multi-level error detection and correction technique for data stored on storage medium [abstract, fig. 1, col. 2, lines 39-47] comprising capability of:

- a storage array coupled to the interconnect and configured to store data received from the host computer system over the interconnect [fig. 1, col. 3, line 23];

In addition, Bruckert explicitly teaches:

- Error processing in a fault tolerant computing system [abstract, fig. 1, col. 1, lines 5-10];

comprising:

- a removable processor and memory modules used to support the error detection and correction system [col. 28, lines 50-61].]

- a client/server data networking environment used within interprocessor and intermodule communication [col. 22, lines 42-49 and col. 28, lines 1-20].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply the a removable processor and memory modules and the client/server data communication environment as taught by Brucket in conjunction with the multi-level error detection and correction technique for data stored on storage medium as disclosed by McAuliffe in order to support the errors notification locally or remotely (i.e., in-band or out-of-band). In addition, by utilizing the Brucket's removable devices, such as data processor and memory, the errors or failure of failed devices can be tracked, isolated, and corrected properly in order to improve the system operation.

As per claims 37-38:

McAuliffe further teaches:

- an amount by which the rate is reduced depends on a number of the plurality of processors that are currently enabled in the data integrity device [col. 2, lines 48-56];

As per claim 39:

This claim is similar to claim 1. The only minor different is that claim 39 introduced a limitation of "a user level of error protection" instead of "a first and second level of error protection" as described in claim 1. However, these limitations are described and performed the same function within the error detection and correction therein. Therefore, this claim is also rejected under the same rationale applied against claim 1. **In addition, all of the limitations have been noted in the rejection as per claim 1.**

As per claim 40-48 and 52-61:

These claims are similar to claims 1-9, 19-27, 29-38. The only minor different is that claim 40 introduced a limitation of "matching results for error indication" instead of "a first and second level of error protection" as described in claim 1. However, McAuliffe and Bruckert do explicitly teach these

limitations via ECC and CRC comparison therein. Therefore, this claim is also rejected under the same rationale applied against claims 1-9, 19-27, 29-38. **In addition, all of the limitations have been noted in the rejection as per claim 1-9, 19-27, 29-38.**

As per claim 62-64:

Due to the similarity of claims 62-64 to claims 1-9 except for a method for performing data integrity comprising a host computer, a storage array, data transferring communication instead of a data processing system comprising host computer system, a storage arrays, an interconnectivity system, etc… etc…; therefore, this claim is also rejected under the same rationale applied against claims 1-9. **In addition, all of the limitations have been noted in the rejection as per claims 1-9.**

As per claim 66:

Due to the similarity of claim 67 to claim 1, therefore, this claim is also rejected under the same rationale applied against claim 1. **In addition, all of the limitations have been noted in the rejection as per claim 1.**

As per claim 67:

Due to the similarity of claim 67 to claim 1 except for a data processing system means comprising host computing means, storage means, communication means, etc… instead of a data processing system comprising host computer system, storage arrays, an interconnectivity system, etc… etc…; therefore, this claim is also rejected under the same rationale applied against claim 1. **In addition, all of the limitations have been noted in the rejection as per claim 1.**

Allowable Subject Matter

7. Claims 10-18, 20, 28, 49-51, and 65 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can

normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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